Abstracts

Chip design for monobit receiver

D.S.K. Pok, C.-I.H. Chen, J.J. Schamus, C.T. Montgomery and J.B.Y. Tsui. "Chip design for monobit receiver." 1997 Transactions on Microwave Theory and Techniques 45.12 (Dec. 1997, Part II [T-MTT] (1997 Symposium Issue)): 2283-2295.

A design for the monobit-receiver application-specific integrated circuit (ASIC) will be described. The monobit receiver is a wide-band (1-GHz) digital receiver designed for electronic-warfare applications. The receiver can process two simultaneous signals and has the potential for fabrication on a single multichip module (MCM). The receiver consists of three major elements: a nonlinear RF front end, a signal sampler and formatting system (analog-to-digital converter (ADC) and demultiplexers), and a patented "monobit" algorithm implemented as an ASIC for signal detection and frequency measurement. The receiver's front end, ADC, and algorithm experimental performance results were previously presented. The receiver uses a 2-b ADC operating at 2.5 GHz whose outputs are collected and formatted by demultiplexers for presentation to the ASIC. The ASIC has two basic functions: to perform a fast Fourier transform (FFT) and to determine the number of signals and report their frequencies. The ASIC design contains five stages: the input, the FFT, the initial sort, the squaring and addition, and the final sort. The chip will process the ADC outputs in real time, reporting detected signal frequencies every 102.4 ns.

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